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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,868	12/27/2001	Tae-Sub Chang	9903-031	2257

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EXAMINER
PATEL, ISHWARBHAI B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 10/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/040,868	CHANG ET AL.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) 23-27 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 27 December 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election / Restriction

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-22, drawn to a substrate, classified in class 174, subclass 262.

   II. Claims 23-27, drawn to a method of forming a substrate, classified in class 29, subclass 852.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions groups II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process such as instead of forming a pattern layer on the insulating layer, patterns can be formed directly on the insulating layer. Furthermore, instead of forming a ground layer on an insulating layer, a laminated insulated board with conductive layer can be used.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, and the

search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Limei Zermilya on August 30, 2002 a provisional election was made without traverse to prosecute the invention of group I, claims 1-22. Affirmation of this election must be made by applicant in replying to this Office action. Claims 23-27 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

6. The drawings are objected to because figures are improperly cross hatched. All of the parts shown in section, and only those parts, must be cross hatched. The cross hatching patterns should be selected from those shown on page 600-81 of the MPEP based on the material of the part. See also 37 CFR 1.84(h)(3) and MPEP 608.02.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

7. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "signal pattern electrically interconnected to the semiconductor chip" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

9. Claims 1-4, 6-8,14-15, 17-19 and 21-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al., US Patent 6,218,731, hereafter Huang.

Regarding claim 1 and 14, Huang discloses a substrate for electrically interconnecting a semiconductor chip mounted thereon to an external device, the substrate comprising:

a ground plane electrically interconnected to a ground power of the semiconductor chip (ground plane 166, see figure 5, column 5, line 46-47);

an insulating layer attached to the ground plane (insulation layer 168, see figure 5, column 5, line 25-30); and

a pattern layer attached to the insulating layer, pattern layer comprising a signal pattern electrically interconnected to the semiconductor chip (pattern layer 174 with traces 175), and

further comprising a ground pattern electrically interconnected to the ground plane, wherein the ground pattern comprises a bonding land, and the bonding land comprising a first via hole configured to electrically interconnect the ground pattern to the ground plane (ground pattern on layer 174 with bond pad 175a).

Regarding claim 14, Huang further discloses all the features of the claimed invention including as shown above including the semiconductor chip, chip 116.

Regarding claim 2, Huang further discloses the first via comprise a blind via, see figure 5.

Regarding claim 3, Huang further discloses a bonding wire electrically coupling the semiconductor chip to the bonding land, see figure 5.

Regarding claims 4 and 15, Huang further discloses the bonding wire is bonded to the first vial hole, see figure 5.

Regarding claims 6 and 17, Huang further discloses the first via hole with inner surface plated with metal, (the via 112 comprises a conductive filling material 110 wrapped with an electroplating layer 108, column 5, line 54-55.

Regarding claims 7 and 18, Huang further discloses solder ball land with solder ball attached to it, see figure 5.

Regarding claims 8 and 19, Huang further discloses a second via electrically interconnected to the ground plane, see figure 5.

Regarding claim 21, Huang further discloses the exposed surface of the semiconductor is covered by an encapsulant, see figure 5.

Regarding claim 22, Huang further discloses the semiconductor chip is attached to the substrate by elastic adhesive, (adhering material 122, column 5, line 1-10).

10. Claims 5, 10-13, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al., US Patent 6,218,731, hereafter Huang, as applied to claims 1-4 above.

Regarding claims 5, 16, though Huang discloses the via coated with copper layer and filled with conductive filler, does not explicitly disclose the filler is a metal. However via filled with metal is known in the art for better electrical connection as well as robust mechanical connections. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of Huang with via filled with metal in order to have better electrical and mechanical connection.

Regarding claim 10, though Huang discloses copper used for both ground and pattern layer, does not explicitly disclose a polyimide tape as an insulation layer. However the use of polyimide tape as an insulator is known in the art for good adhesion and relative flexibility and can be used depending upon the specific requirement. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of Huang with polyimide tape as an insulation layer. Furthermore, it has been held to be within the general skill in the art to

select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding claims 11 and 12, the applicant is claming how the substrate is formed, which is a process limitation. Such a process limitation defines the claimed invention over the prior art only to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art, in the case that the product is the same as, or obvious over the prior art. *In re Thorpe,* 227 USPQ 964, 966 (Fed. Cir. 1985).

Regarding claim 13, Though Huang is not disclosing the wafer level package; such use of substrate for wafer level package is known in art and can be used for any other type of semiconductor package depending upon a specific requirement. Further, it has been held that the recitation that an element is "adapted to' perform a function is not a positive limitation but only require the ability to so perform. It does not constitute a limitation in patentable sense. *In re Hutchison*, 69 USPQ 138.

11. Claims 9 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al., US Patent 6,218,731, hereafter Huang as applied to claims 1-4 above, and further in view of Lau et al., US Patent 6,057,601, hereafter Lau.

Regarding claim 9 and 20, though Huang does not disclose ground plane split into first and second ground plane, such splitting is known in the art to have flexibility in selecting the ground / power connection depending upon specific layout of signal input /output of the semiconductor device. Lau discloses one such substrate with split ground plane. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of Huang with split ground plane as taught by Lau in order to have greater flexibility in selecting the ground power.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bhatt et al., Brooks et al., Terui, Asada et al., Ito, Fazelpour, Yew et al., and Huang et al., disclose assembly similar to applicant's claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (703) 305 2617. The examiner can normally be reached on M-F (6:30 - 4) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L Talbott can be reached on (703) 305 9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305 3431 for regular communications and (703) 305 7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956.

ibp
September 26, 2002

Albert W. Paladini 9-27-02
ALBERT W. PALADINI
PRIMARY EXAMINER